a ferroelectric capacitor having first and second terminals, the first terminal coupled to a drain of the enhancement mode transistor and the second terminal coupled to a cell plate, for storing data.

5. (Twice Amended) A ferroelectric random access memory (FeRAM) device including a plurality of ferroelectric memory cells, comprising:

first active areas incorporating therein gates of depletion mode transistors and operating as bit lines;

second active areas adjacent to the first active areas incorporating therein gates of enhancement mode transistors;

word lines coupled to the gates of the depletion mode transistors and the gates of the enhancement mode transistors; and

ferroelectric capacitors each having first and second terminals, the first terminal coupled to a drain of a corresponding transistor of the enhancement mode transistors and the second terminal coupled to a common cell plate, for storing data.

Please add new claims 10-14 to read as follows:

--10. (New) A ferroelectric random access memory (FeRAM) having a plurality of ferroelectric memory device, each ferroelectric memory cell comprising:

a depletion mode transistor having a first drain/source and a second drain/source, wherein the first drain/source is coupled to a drain/source of a depletion mode transistor of another ferroelectric memory cell to be operated as a bit line;

an enhancement mode transistor having a third drain/source, a fourth drain/source extended to the first drain/source of the depletion mode transistor;

a word line commonly coupled to a gate of the depletion mode transistor and a gate of the enhancement mode transistor; and

a ferroelectric capacitor having first and second terminals, the first terminal coupled to the third drain/source of the enhancement mode transistor and the second terminal coupled to a cell plate, for storing data.

11. (New) Each ferroelectric memory cell as recited in claim 10, wherein the bit line is parallel with a cell plate line of the ferroelectric capacitor.

12. (New) Each ferroelectric memory cell as recited in claim 11, wherein the first drain/source of the depletion mode transistor and the fourth drain/source of the enhancement mode transistor are n-type.

13. (New) Each ferroelectric memory cell as recited in claim 13, wherein the third drain/source of the enhancement mode transistor is n-type.

14. (New) The ferroelectric random access memory (FeRAM) of claim 10, further comprising a sense amplifier for sensing and amplifying data applied to the bit line to generate an amplified signal.--